REMARKS

Claims 2-11 again stand rejected only under 35 U.S.C. 102(e) as being unpatentable over Ikeda et al. (U.S. 5,815,136). Applicant respectfully traverses this rejection for the reasons of record, and as follows.

Applicant maintains and incorporates by reference herein those arguments previously advanced on pages 2 through 11 of Response F, filed December 2, 2003. Applicant respectfully requests that the Examiner reconsider those arguments, and withdraw the outstanding Section 102 rejection. Additionally, Applicant respectfully requests that the Examiner consider the following new arguments, and expansion upon the previous arguments.

On page 2 of the outstanding Office Action, the Examiner again asserts that "the CPU [of Ikeda's] Fig. 16 (1601) which may include a lot of memories which is different from the main memory [also of Ikeda's] Fig. 16 (1602) corresponding to memories which store information for controlling displaying of the data of the image." This assertion though, does not consider all of the recited language from independent claim 2 of the present invention, for example.

As last amended, claim 2 of the present invention clearly features, among other things, that an address bus supplies address signals for selecting one of the memories at issue. Applicants note that the Examiner appears to have not considered this particular feature of the present invention, in rejecting claim 2 based upon Ikeda alone. In fact, Ikeda fails to

teach or suggest any such features, and even teaches the opposite. Even if the Examiner were correct in his assertion that the CPU 1601 of Ikeda could contain memories for storing display control information (which Applicants do not concede), Ikeda clearly shows that memories/registers provided within the CPU 1601 are not accessible or selectable through the address bus 1604. Ikeda otherwise describes nothing in the corresponding text to contradict the clear showing on Fig. 16. For at least these additional reasons then, the Section 102 rejection based on Ikeda is again respectfully traversed.

The Examiner then cites (page 5 of Paper no. 22) to the buffer 1609 as an example for the storage of information for controlling display data, but the text of Ikeda does not support this assertion either. The Examiner's own statements (same page) recognize that Ikeda's "numeral 1609 denotes a buffer for display data." (Emphasis added). As repeatedly pointed out by Applicant, and even recited in the claims of the present invention, display data is not the same as information for controlling the display data. Furthermore, Fig. 16 of Ikeda shows that the buffer 1609 is connected only to the data bus 1605, and not the control signal bus 1606, or even the address bus 1604. The Examiner appears to even recognize that Fig. 16 of Ikeda shows that the data bus (1605) and the address bus (1604) of Ikeda "are not included in the control signal bus [1606], which control the system." (Page 6 of Paper No. 22). Accordingly, for these further reasons as well, the Section 102 rejection is traversed.

The Examiner next, on page 6 of Paper No. 2, asserts that display control information must be "*inherently* transmitted through the address bus." However, this stated

rationale for inherency is contradicted by the Examiner's immediately preceding remarks, that "the address bus [is] not included in the control signal bus, which control[s] the system." The Examiner should therefore withdraw his assertion of inherency, in that he has provided no objective evidentiary support for the claim, and because it is contradicted by the plain text of the Ikeda reference, as well as the Examiner's own, other assertions.

Applicant otherwise respectfully requests that the Examiner cite to some objective support, other than his own personal assertions, that the address bus must inherently transmit display control information. As taught by Ikeda, however, the address bus 1605 transmits address information, and not information for controlling the display of image data. (See Fig. 16). After six fully traversed Office Actions, the Examiner should provide some objective support for such a broad assertion, or should withdraw it.

Lastly, the Examiner now implies for the first time, again after six successive Office Actions and Responses, that the "claims are so broad and vague in the way they are written." The Examiner, however, has failed to identify exactly what specifically recited feature(s) in the claims he finds vague or overly broad. Applicant notes that the Examiner has not rejected any single claim under Section 112. Applicant therefore respectfully requests that the Examiner withdraw this statement. One skilled in the art can clearly understand the scope of Applicant's claimed invention when interpreted in light of the Specification.

For all of the foregoing reasons therefore, Applicant submits that this Application, including claims 2-11, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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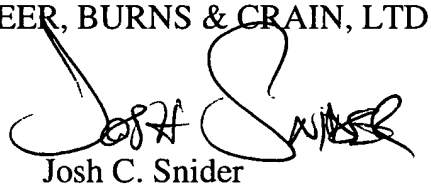
By 

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